A Digital Integrated Circuit at 180 nm Technology to Cope With Solar Cells Partial Shading

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***Abstract*— In this paper, a 4-bit counter and a 16 × 1 multiplexer based on a 180 nm CMOS semiconductor process technology were developed. This digital integrated circuit is necessary to integrate a partial shading condition identification system into photovoltaic panels. The primary focus is to optimize the energy efficiency of these systems. In addition, under partial shading conditions, a bypass is necessary to prevent local overheating due to power dissipation under reverse bias operation. Under these circumstances, thin-film technology, such as from organic semiconductors, may degrade before planned. Therefore, an operating frequency fixed at 32 MHz resulted in a manufacturing layout of 2477 µm², demonstrating efficient compactness for embedded photovoltaic panel control.**

Keywords—CMOS, counter, multiplexer, photovoltaics panels

I. Introduction

The partial shading in photovoltaic panels occurs when some modules are in shadowed areas while others are exposed to direct sunlight. This disparity generates local overheating and, consequently, power dissipation regions, compromising solar panels' lifespan and efficiency [1]. Thin-film technologies such as the ones based on organic semiconductors do not support high-temperature operation. Local overheating may lead to breaking carbon-to-carbon sp^2 bonds and loss of conductivity by creating charge traps [2]. In addition, these traps tend to be deep in energy levels, slowing down time transients and decreasing electric current conduction capability [3,4]. Faced with this issue, the design of a partial shading identification system has been proposed, comprising the implementation of components such as logic gates, oscillators, multiplexers, flip-flops, and counters.

In the digital design, each signal originating from the solar panel modules is connected to the inputs of the multiplexer, whose selector bits are defined by the outputs of a counter synchronized by the oscillator. This arrangement enables an automatic, systematic, and continuous scan of the photovoltaic solar cells from the panel, detecting adverse behaviors that could compromise the system.

In this context, this paper features the development of a 4-bit counter and a 16 × 1 multiplexer with high operating frequency and low power consumption, suitable for 180 nm technology. Details on the analog integrated circuitry, such as operational amplifier-based comparators design, will be discussed and shared in future publications.

II. Materials and Methods

A. Implementation of the 4-bit Counter

To simplify the circuit of the 4-bit counter, D flip-flops were chosen based on a master-slave connection [5]. Consequently, a D flip-flop sensitive to the rising edge of the clock signal is obtained. Additionally, pause and reset functions were carefully added, identified as Enable (*E*) and Reset (*R*) control signals, respectively. To ensure robustness and proper operation, the counter must operate synchronously. Therefore, a simple multiplexer logic was implemented to the *D* input of the flip-flop [6], following the behavior described in Table I. Note that *Y* is the output of the multiplexer, *Q* is the counter output, and *D* is the current given value at the input.

TABLE I. Truth Table of the Multiplexer Logic (X = don't care).

E	***R***	***D***	***Y***
0	X	X	Qn
1	0	X	D
1	1	X	0

The counter has a truth table, described as follows:

$$Qn = Z \Rightarrow Q(n+1) = Z + 1 \quad (1)$$

where counting starts from $Z = 0$ and progresses to the maximum count value of $Z = 15$, following a cyclic sequence [7]. Based on this, it is possible to perform minimization using the Karnaugh Map, resulting in combinational circuits described by the following expressions:

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$$D3 = Q3 \oplus Q2Q1Q0 \quad (2)$$

$$D2 = Q2 \oplus Q1Q0 \quad (3)$$

$$D1 = Q1 \oplus Q0 \quad (4)$$

$$D0 = Q0' \quad (5)$$

where *Dn* is the *D* input of flip-flop n, and *Qn* is the output of flip-flop n [8].

B. Implementation of the 16 × 1 Multiplexer

The multiplexer was implemented according to [4]. Since it has 4 selector bits (number of counter outputs connected), it was designed for a 16-channel input operation, reaching its maximum capability.

The multiplexer transmits one of its inputs depending on the selector bits according to the following logic:

$$(S_3S_2S_1S_0)_2 = (S)_{10} \Rightarrow Y = I_S \quad (6)$$

where $S_3S_2S_1S_0$ are the 4 selector bits, *S* is its equivalent decimal value, *Y* is the multiplexer output, and *I* is the multiplexer input.

Even though it results in a larger IC area, it was decided to use transmission gates, i.e. NMOS and PMOS parallel association, to allow analog signal transmission. This is necessary since the multiplexer is connected directly to the solar panels and, consequently, to analog signals. Additionally, this design choice also ensures that the signal has lower propagation delays and a full ground (GND) to positive source bias (VDD) range.

C. Circuit Sizing and Simulation Tools

A Generic Process Design Kit (GPDK) of 180 nm was used in the software Virtuoso Cadence®, where NMOS and PMOS transistors have the same k_n and k_p parameter values. Additionally, this GPDK defines a minimum width (*W*) of 400 nm. Therefore, $Wn = Wp = 400$ nm was chosen for the inverters, which served as the basis for impedance matching for the rest of the circuit.

III. Results and Discussions

A. Simulation of the 4-bit Counter

The implemented circuit diagram for the D flip-flop is shown in Fig. 1. It forms the foundational building block for the 4-bit counter, ensuring reliable and accurate state transitions. The design has been tested to verify its performance and stability, confirming its suitability for integration into the overall system architecture.

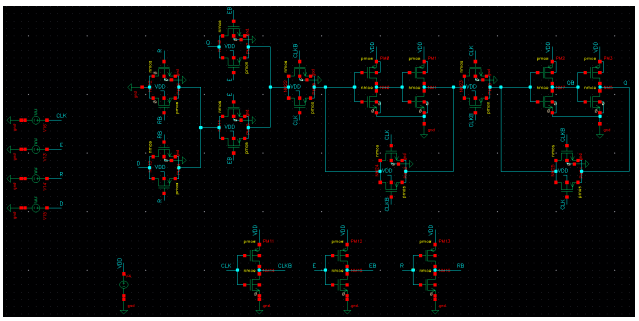

Fig. 1. Schematic of Flip-flop D from software Virtuoso Cadence®.

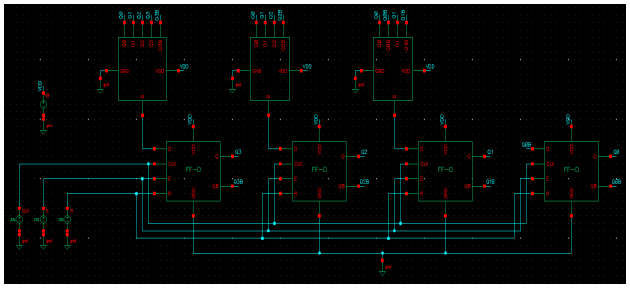

Fig. 2. Schematic of 4-bit counter from software Virtuoso Cadence®.

Fig. 2 shows the implementation of the 4-bit counter diagram, such as the logical connections and structure, as provided in [5]. Fig. 3 shows their respective characteristic curves fo a simulation at an operating frequency of 32 MHz. These simulations validate the counter's performance, demonstrating its accuracy and reliability in application, and providing critical insights into its dynamic behavior under typical operating conditions.

After validating the 4-bit counter through the previous simulation, the originated fabrication layout is given in Fig. 4. This circuit has dimensions of 43.2 µm × 32.3 µm, featuring an area of 1395 µm². The compact size of the design ensures efficient use of silicon CMOS technology, which is crucial for integrating multiple components in a constrained space while maintaining high performance and reliability in practical applications.

B. Simulation of the 16 × 1 Multiplexer

The implemented circuit diagram for the 16 × 1 multiplexer is shown in Fig. 5. It was based on logic circuits in [4]. This implementation involves a careful design process to ensure that the multiplexer can effectively select one of its sixteen input channels based on the 4-bit selector inputs. The diagram showcases the logical arrangement and interconnections of the multiplexer's components, which have been optimized for performance and efficiency, within the system's operating parameters.

Fig. 6 shows all the multiplexer inputs, which are DC levels ranging from GND to VDD, chosen through the selector bits. These inputs are sequentially selected based on the 4-bit selector inputs. These plots provide a clear visualization of how the multiplexer operates, demonstrating its ability to accurately choose one of the sixteen input levels according to the binary value of the selector bits. This critical functionality ensures precise signal control, guaranteeing reliable system performance.

After validating the 16 × 1 multiplexer through the previous simulation, the created fabrication layout is provided

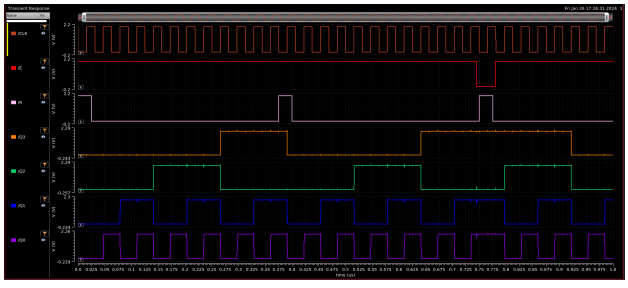

Fig. 3. Characteristic curves of the 4-bit counter from software Virtuoso Cadence®.

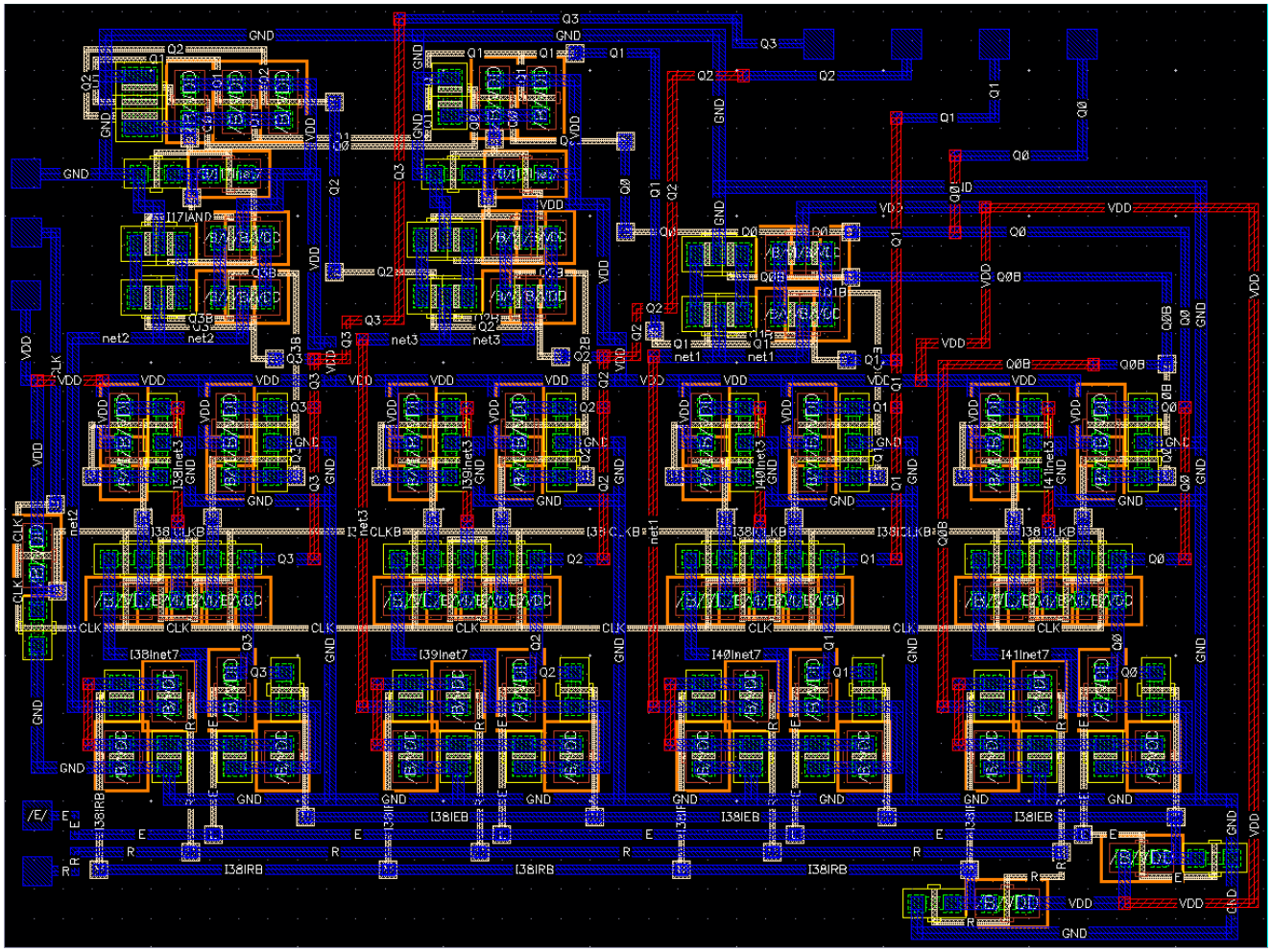

Fig. 4. Fabrication layout of the 4-bit counter from software Virtuoso Cadence®.

Fig. 7. This circuit has dimensions of 32.3 µm × 33.5 µm, featuring an area of 1082 µm². The compactness of the layout highlights its effective space utilization, which is crucial for accommodating numerous components within a constrained area while ensuring optimal performance and reliability.

C. *Next Steps*

This work was fully performed as undergraduate research within the Electrical Engineering Course of the State University of Campinas (UNICAMP) in Brazil. In future work, the counter and the multiplexer will be integrated with a ring oscillator for clock signal generation. In addition, it will feature operational amplifiers for analog signal processing, such as the implementation of voltage comparators, as well as bypassing circuits for the devices under shading conditions. In addition, tracking partial shading is also relevant for applications such as floating solar and improving output power in PV installations. Finally, due to higher fabrication availability and reasonable costs for academia, the design will be migrated from the 180 nm GPDK to the 65 nm technology from Taiwan Semiconductor Manufacturing Company (TSMC).

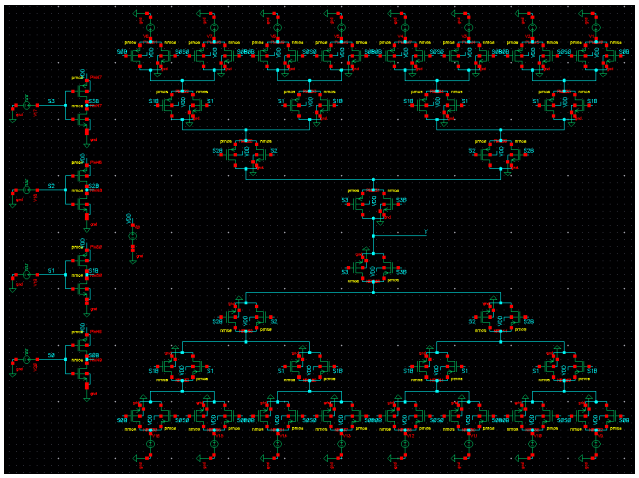

Fig. 5. Schematic of 16 × 1 multiplexer from software Virtuoso Cadence®.

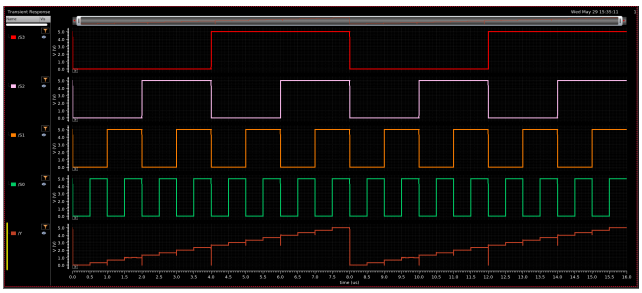

Fig. 6. Characteristic curves of the 16 × 1 multiplexer from software Virtuoso Cadence®.

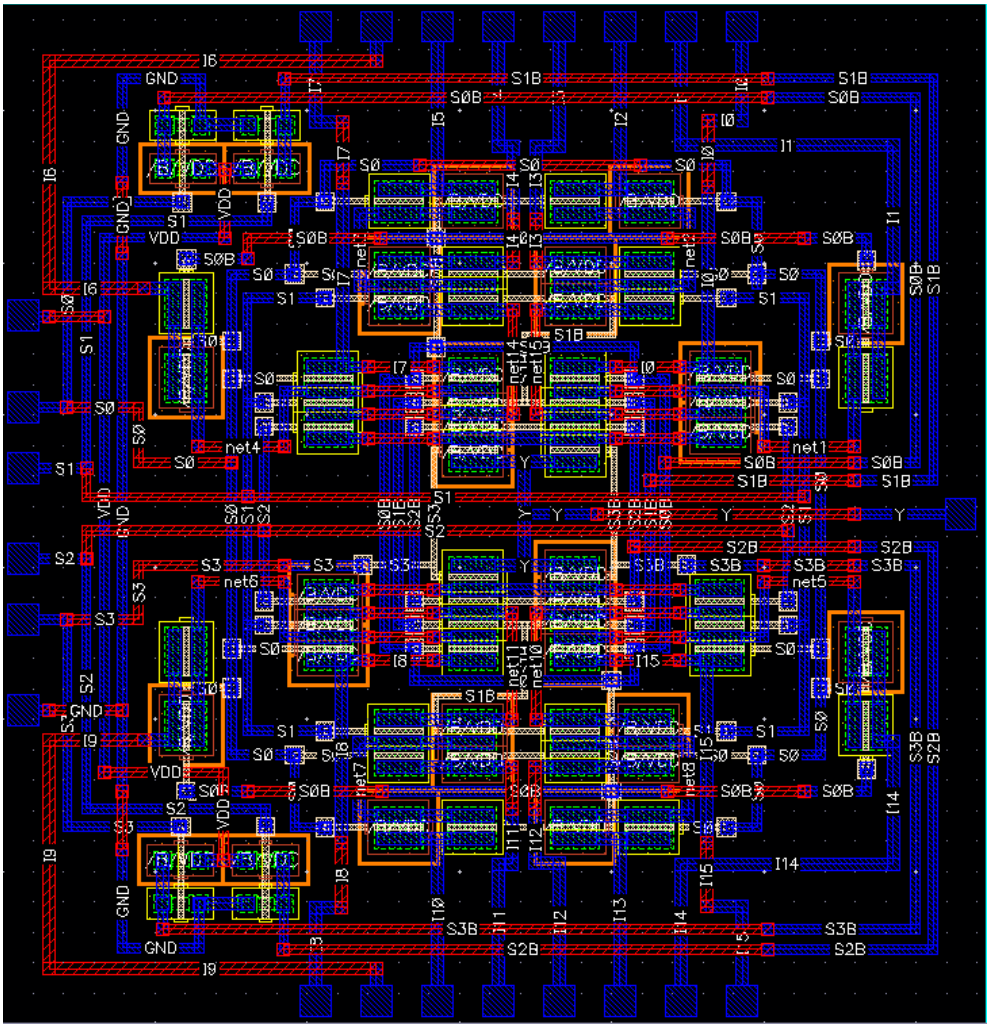

Fig. 7. Fabrication layout of the 16 x 1 multiplexer from software Virtuoso Cadence®.

IV. Conclusions

The 4-bit counter demonstrates counting capability from 0 to 15 in decimal. Notably, it exhibits robust responsiveness to both Enable and Reset control signals, even under the demanding operational conditions of a 32 MHz frequency. The presented counting capability can be expanded through circuit cascading, enabling the construction of counters with a greater number of bits.

The 16 × 1 multiplexer admits values in a voltage range from GND to VDD, guaranteeing compatibility with analog signals such as the one from a solar cell. Additionally, it has a fast transmission response, as expected.

In conclusion, this work represents one more step towards an integrated circuit to cope with solar cell operation under partial shading conditions, as discussed in [1-3]. By enhancing the functionality and performance of essential components such as the 4-bit counter and 16 × 1 multiplexer, this work lays the foundation for more efficient and robust PV panel optimization strategies.

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